WHAT IS CLAIMED IS:

1. A microelectronic assembly comprising:

a microelectronic element having a front face including contacts, a back surface remote therefrom and edges extending therebetween;

a mass of a dielectric material at least partially encapsulating said microelectronic element;

conductive units embedded in said mass of dielectric material along at least one microelectronic element edge, at least some of said conductive units being exposed on oppositely-facing exterior surfaces of said mass of dielectric material; and

conductive elements extending through said mass of dielectric material and electrically interconnecting said contacts with said conductive units.

2. The assembly as claimed in claim 1, wherein said mass of dielectric material has a top exterior surface juxtaposed with said front face of said microelectronic element and a bottom exterior surface juxtaposed with said back surface of said microelectronic element, at least some of said conductive units being exposed at both said top and bottom exterior surfaces of said dielectric material.

3. The assembly as claimed in claim 2, wherein at least some of said conductive units include pad portions exposed at said bottom surface of said dielectric material and a protrusion extending from said pad portion exposed at said top surface of said dielectric material, wherein the cross sectional area of each said protrusion is smaller than the cross sectional area of the pad portion associated with such protrusion.

4. The assembly as claimed in claim 3, wherein each of said protrusions extends from a portion of the associated pad portion furthest from said microelectronic element.

5. A microelectronic device including first and second microelectronic assemblies as claimed in claim 2,

wherein said assemblies are juxtaposed with each other such that exposed conductive units at said bottom exterior surface of said first assembly are electrically connected to said exposed conductive units at said top exterior surface of said second assembly.

6. The assembly as claimed in claim 5, further comprising a substrate underlying said bottom exterior surface of said second assembly, wherein said exposed conductive units of said second assembly are connected to said substrate.

7. The assembly as claimed in claim 2, wherein said conductive units protrude from said top exterior surface or said bottom exterior surface or both.

8. The assembly as claimed in claim 1, wherein said back surface of said microelectronic element is exposed at an exterior surface of said assembly.

9. The assembly as claimed in claim 8, further comprising thermally conductive adhesive attached to said back surface of said microelectronic element.

10. The assembly as claimed in claim 1, wherein at least some of said conductive units have hollow centers.

11. The assembly as claimed in claim 10, wherein said hollow centers extend through said at least some conductive units.

12. The assembly as claimed in claim 10, further comprising a reflowable electrically conductive material disposed within the hollow centers of said conductive units.

13. The assembly as claimed in claim 12, wherein said reflowable material is exposed at least one exterior surface of the assembly.

14. A microelectronic assembly comprising:

a first microelectronic element having a front face including contacts and a back surface remote therefrom;

a second microelectronic element juxtaposed with said front face of said first microelectronic element and having terminals thereon;

a mass of a dielectric material at least partially encapsulating said first microelectronic element and fully encapsulating said second microelectronic element;

conductive units secured to said mass of dielectric material; and

conductive elements extending through said mass of dielectric material and electrically interconnecting said contacts and said terminals with said conductive units and/or with each other, wherein one or more of said conductive units are exposed at an exterior surface of said assembly.

15. The assembly as claimed in claim 14, wherein said second microelectronic element includes a face surface having terminals and a back surface remote therefrom.

16. The assembly as claimed in claim 15, wherein said back surface of said second microelectronic element faces said front surface of said first microelectronic element.

17. The assembly as claimed in claim 15, wherein said back surface of said second microelectronic element is attached to said front surface of said first microelectronic element.

18. The assembly as claimed in claim 17, wherein said conductive elements interconnect at least one of said terminals to at least one of said contacts.

19. The assembly as claimed in claim 17, further comprising thermally conductive adhesive attached to said back surface of said first microelectronic element.

20. The assembly as claimed in claim 14, wherein said back surface of said first microelectronic element is exposed at an exterior surface of said assembly.

21. A method of making a semiconductor chip package, comprising the steps of:

providing a first sacrificial layer;

providing a dielectric base material on the first sacrificial layer;

providing an array of conductive pads on said dielectric base material such that a central region is defined by the pads;

attaching a back surface of a semiconductor chip to the first sacrificial layer within the central region so that a contact bearing surface of the chip faces away from the first sacrificial layer;

electrically connecting each contact to a respective pad;

providing a second sacrificial layer juxtaposed with the contact bearing surface of the chip;

depositing curable dielectric material such that the electrical connections and the chip are each encapsulated and curing the dielectric material;

forming apertures extending between the first and second sacrificial layers, at least some of said apertures extending through the cured dielectric material, through at least some of said conductive pads and through the dielectric base material;

depositing a conductive metal in said apertures so as to form conductive vias extending between the sacrificial layers, at least some of said conductive vias being electrically connected to at least some of said conductive pads; and

removing at least a portion of each said sacrificial layer.

22. The method as claimed in claim 21, wherein said step of depositing a conductive metal is performed so as to form flange portions projecting outwardly from said conductive vias over the sacrificial layers.

23. The method as claimed in claim 22, wherein said removing is performed so as to remove the entirety of said sacrificial layers other than portions of said layers covered by said flange portions.